O.P.Code:23CS0506	R23	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech.II Year II Semester Regular Examinations July/August-2025

DIGITAL LOGIC AND COMPUTER ORGANIZATION

(Common to CAD, CSM & CAI)

Time: 3 Hours **Max. Marks: 70**

PART-A

(Answer all the Questions **10 x 2 = 20** Marks)

1	a	Conver binary number $(1011000.110)_2$ to octral number.	CO1	L2	2M
	b	What meant by universal gates.	CO1	L1	2M
	c	Define the sequenctial circuit.	CO1	L1	2M
	d	Sketch the basic functional units of computer.	CO3	L2	2M
	e	Represent -7 in signed magnitude, 1s complement and 2s complement.	CO2	L3	2M
	f	What is the need of multiple organization?	CO3	L2	2M
	g	What is the need of memory?	CO5	L2	2M
	h	What is cache memory?	CO5	L1	2M
	i	Define debugging.	CO6	L1	2M
	j	Classify interface circuits.	CO6	L1	2M

PART-B

(Answer all Five Units **5 x 10 = 50** Marks)

UNIT-I

2	a	Simplify the following Boolean expressions using K-map i) F (x, y, z) = Σm (2, 3, 4, 5) ii) F (x, y, z) = Σm (3, 4, 6, 7)	CO1	L1	5M
	b	Explain about Basic Logic gates with symbols and truth table.	CO1	L2	5M
		OR			
3	a	Design full adder using two half adders and OR gate.	CO2	L4	5M
	b	Represent signed numbers from +7 to -8 using different ways of representation.	CO1	L2	5M

UNIT-II

4	a	Define a Register. Explain in detail about various Shift Registers.	CO1	L1	5M
	b	Explain briefly about the multiprocessors and multi computers of a computer.	CO2	L2	5M
		OR			
5	a	Explain the working principle of T and D flip-flops.	CO1	L2	5M
	b	Describe the Basic Operational Concepts of computer with neat diagram.	CO3	L2	5M

UNIT-III

6	a	Explain the Flow chart for Addition and Subtraction.	CO3	L2	5M
	b	Develop and discuss the Flow chart for Division of numbers Give the step-by-step procedure to Divide 11 with 3 and find the results.	CO1	L6	5M
		OR			
7	a	Explain the working of a Ripple carry adder.	CO1	L2	6M
	b	What is Hardwired Control? Explain in detail with a neat diagram.	CO4	L2	4M

UNIT-IV

8	a	Distinguish between SRAM & DRAM.	CO5	L2	6M
	b	What are the performance considerations in cache memory?	CO5	L2	4M
		OR			
9	a	Describe in detail about the memory management requirements.	CO5	L1	5M
	b	Compare the various cache mapping techniques.	CO5	L2	5M

UNIT-V

10	a	Explain the interrupts in input/output organization.	CO6	L3	5M
	b	Draw the PCI bus architecture and explain its operation.	CO6	L1	5M
		OR			
11	a	Give detailed notes on DMA transfers with neat sketch.	CO6	L2	5M
	b	Explain the standard I/O devices.	CO6	L2	5M

***** END *****